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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/777,693	KOYAMA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,19-27,36-45,54-61 and 71-123* is/are pending in the application.

4a) Of the above claim(s) *1-10,36-45,54-61,71-79 and 88-104* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-27,80-87 and 105-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the newly introduced limitation of independent claims 19,80,105 and 115: "a plurality of enabling circuits which limit output periods of the plurality of storage circuits" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

the newly introduced limitation of independent claims 19,80,105 and 115: "a plurality of enabling circuits which limit output periods of the plurality of storage **converter** circuits" is not disclosed in the specification.

Notice, that on page 12, Lines 17-19 no storage **converter** circuits and no description what kind of limiting of an output period is implemented.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 19-27,80-87 and 105-123 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The newly introduced limitation of independent claims 19,80,105 and 115: "a plurality of enabling circuits which limit output periods of the plurality of storage **converter** circuits" is not disclosed in the specification or shown in Figures.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 19-27,80-87 and 105-123 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what is "...storage **converter** circuits..." in the newly introduced limitation of independent claims 19 and what kind of limiting of an output period is implemented for independent claims 19,80,105 and 115?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 19, 25, 80, 86-87, 105-106, 112, 115-116, 122-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya (US Patent No.5,170,158) in view of Lewis (US Patent No. 5,589,847) and Yoshida et al. (Pub. No.: US 2006/0132420 A1).

As to claim 19, as best understood by examiner, Shinya teaches an image display device (See Col, 1, Lines 6-10), comprising:

a pixel array portion including a plurality of signal lines (See Fig. 1, item 2), a plurality of scan lines (See Fig. 1, item 3), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines

intersect with each other (See Fig. 1, item 4), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 1, item 5, Col. 1, Lines 21-30);

a signal line driver circuit for driving the plurality of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32); and

a scan line driver circuit for driving the plurality of scan lines (See Fig. 1, item 7, Col. 1, Lines 32-39),

wherein signal line driver includes an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit (m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23).

the first example of Shinya does not disclose a plurality of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different

examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

Shinya does not disclose an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

Lewis teaches an operation in which the digital picture signals are inputted to the respective shift registers (Fig. 15A, items Digital data in, 505), the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits (Fig. 15A, item 515), and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped (See Fig. 15B, items SR Clock, LATCH), is repeated n (n is an integer not less than 2) (See Fig. 15B, items SELECT 1, SELECT 2,...) times in a time corresponding to one horizontal scan period (See Figs. 15A-15B, items SR CLOCK, LATCH, Col. 10, Lines 22-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Lewis into Shinya system in order to fabricate from polysilicon (See Col. 4, Lines 41-45 in the Lewis reference).

Shinya and Lewis do not disclose a plurality of enabling circuits which limit output periods of the plurality of storage circuits.

Yoshida et al. teaches a plurality of enabling circuits which limit output periods of the plurality of storage circuits (See Figs. 1 and 3A-3F, items 8,10,oe,12,13, paragraph 0062).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Yoshida et al. into Lewis and Shinya system in order to reduce load to D/A converter and power consumption (See paragraph 0017 in the Yoshida et al. reference).

As to claim 80, as best understood by examiner, Shinya teaches a signal driver circuit of an image display device (See Col, 1, Lines 6-10) for driving the plurality of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32), the signal line driver circuit comprising:

an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit (m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (see Fig. 2, items P1-Pn, Col. 4, Lines 16-23),

The first example of Shinya does not disclose a plurality of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

Shinya does not disclose an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

Lewis teaches an operation in which the digital picture signals are inputted to the respective shift registers (Fig. 15A, items Digital data in, 505), the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits (Fig. 15A, item 515), and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped

(See Fig. 15B, items SR Clock, LATCH), is repeated n (n is an integer not less than 2) (See Fig. 15B, items SELECT 1, SELECT 2,...) times in a time corresponding to one horizontal scan period (See Figs. 15A-15B, items SR CLOCK, LATCH, Col. 10, Lines 22-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Lewis into Shinya system in order to fabricate from polysilicon (See Col. 4, Lines 41-45 in the Lewis reference).

Shinya and Lewis do not disclose a plurality of enabling circuits which limit output periods of the plurality of storage circuits.

Yoshida et al. teaches a plurality of enabling circuits which limit output periods of the plurality of storage circuits (See Figs. 1 and 3A-3F, items 8,10,oe,12,13, paragraph 0062).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Yoshida et al. into Lewis and Shinya system in order to reduce load to D/A converter and power consumption (See paragraph 0017 in the Yoshida et al. reference).

As to claim 105, as best understood by examiner, Shinya teaches an image display device (See Col, 1, Lines 6-10), comprising:

a pixel array portion including a k of signal lines (See Fig. 1, item 2), a plurality of scan lines (See Fig. 1, item 3), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines

intersect with each other (See Fig. 1, item 4), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 1, item 5, Col. 1, Lines 21-30);

a signal line driver circuit for driving the k of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32); and

a scan line driver circuit for driving the plurality of scan lines (See Fig. 1, item 7, Col. 1, Lines 32-39),

wherein signal line driver includes an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit (m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and a k/n (in reference N/M) of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23

The first example of Shinya does not disclose a m x k/n of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits (equal to the number of the DAC) for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

Shinya does not disclose an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

Lewis teaches an operation in which the digital picture signals are inputted to the respective shift registers (Fig. 15A, items Digital data in, 505), the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits (Fig. 15A, item 515), and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped (See Fig. 15B, items SR Clock, LATCH), is repeated n (n is an integer not less than 2) (See Fig. 15B, items SELECT 1, SELECT 2,...) times in a time corresponding to one horizontal scan period (See Figs. 15A-15B, items SR CLOCK, LATCH, Col. 10, Lines 22-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Lewis into Shinya system in order to fabricate from polysilicon (See Col. 4, Lines 41-45 in the Lewis reference).

Shinya and Lewis do not disclose a plurality of enabling circuits which limit output periods of the plurality of storage circuits.

Yoshida et al. teaches a plurality of enabling circuits which limit output periods of the plurality of storage circuits (See Figs. 1 and 3A-3F, items 8,10,oe,12,13, paragraph 0062).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Yoshida et al. into Lewis and Shinya system in order to reduce load to D/A converter and power consumption (See paragraph 0017 in the Yoshida et al. reference).

As to claim 115, as best understood by examiner, Shinya teaches a signal driver circuit of an image display device (See Col, 1, Lines 6-10) for driving the k of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) (in reference 8) digital picture signals are inputted, the number of the shift registers being an integral multiple of m (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and

a k/n (in reference N/M) of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23)

The first example of Shinya does not disclose a m x k/n of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits (equal to the number of the DAC) for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

Shinya does not disclose an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

Lewis teaches an operation in which the digital picture signals are inputted to the respective shift registers (Fig. 15A, items Digital data in, 505), the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a

clock signal until they are outputted to the corresponding storage circuits (Fig. 15A, item 515), and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped (See Fig. 15B, items SR Clock, LATCH), is repeated n (n is an integer not less than 2) (See Fig. 15B, items SELECT 1, SELECT 2,...) times in a time corresponding to one horizontal scan period (See Figs. 15A-15B, items SR CLOCK, LATCH, Col. 10, Lines 22-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Lewis into Shinya system in order to fabricate from polysilicon (See Col. 4, Lines 41-45 in the Lewis reference).

Shinya and Lewis do not disclose a plurality of enabling circuits which limit output periods of the plurality of storage circuits.

Yoshida et al. teaches a plurality of enabling circuits which limit output periods of the plurality of storage circuits (See Figs. 1 and 3A-3F, items 8,10,oe,12,13, paragraph 0062).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Yoshida et al. into Lewis and Shinya system in order to reduce load to D/A converter and power consumption (See paragraph 0017 in the Yoshida et al. reference).

As to claim 25, 112, Shinya teaches a display is carried out using a liquid crystal material (see Col. 1, Lines 12-19).

As to claim 106, 116, Shinya teaches the number of converter circuits is 4 (k/8 X 2) (See Fig. 2, item 15, Col. 5, Lines 38-48).

As to claims 86-87,122-123, Lewis teaches the driver circuit is formed of a poly silicon thin film transistor or of a single crystal transistor (See Abstract).

6. Claims 20-24, 81-85, 107-111 and 117-121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya, Lewis and Yoshida et al. as applied to claims 19, 80, 105 and 115 above, and further in view of Luder et al. (US Patent No. 5,642, 117).

As to claim 20, 81, 107 and 117, Shinya, Lewis and Yoshida et al. do not disclose a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Shinya, Lewis and Yoshida et al. system in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 21-24, 82-85, 108-111 and 118-121, Shinya, Lewis and Yoshida et al. do not disclose the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters.

Luder et al. teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Figs. 14A-14B, items Q1-Q2, nQ1-Nq2, 400, 420, 430, Col. 9, Lines 51-67 and Col. 10, Lines 1-21).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Luder et al. into Shinya, Lewis and Yoshida et al. system in order to reduce cost (See Col. 2, Lines 16-19 in the Luder et al. reference).

7. Claims 26, 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya, Lewis and Yoshida et al. as applied to claims 19, 105 above, and further in view of Friend et al. (US Patent No. 5,247, 190).

Shinya, Lewis and Yoshida et al. do not disclose a display is carried out using an electroluminescence material.

Friend et al. teaches a display is carried out using an electroluminescence material (See Fig. 3, items 3-5, Col. 8, Lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to use materials as shown by Friend et al. in Shinya, Lewis and Yoshida et al. system in order to increase the range of applications.

8. Claims 27, 114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya, Lewis and Yoshida et al. as aforementioned in claims 19, 105 in view of Matsueda et al (US Patent No. 6,384,806 B1).

Shinya, Lewis and Yoshida et al. do not teach a portable telephone, which uses the image display device.

Matsueda et al. shows a portable telephone, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Shinya, Lewis and Yoshida et al. apparatus in the portable telephone as shown by Matsueda et al. in order to increase the range of applications.

Response to Arguments

9. Applicant's arguments with respect to claims19-27,80-87,105-123 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
12.27.06

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